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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,104	08/17/2001	Eiji Yoshida	212881US2	3616

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,104	YOSHIDA, EIJI	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,6,8,10-12,15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) *4,8,10,12,15 and 17-19* is/are withdrawn from consideration.

5)☒ Claim(s) *11* is/are allowed.

6)☒ Claim(s) *6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 2/9/2004 forms the basis of this Office Action. In said Amendment Applicant canceled claims 1 and 7 and amended claims 6 and 11. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed 2/9/2004 have been fully considered but they are not persuasive. Although claim 11 has been placed in allowable form by incorporation of the independent (previous and now canceled) claim 1, claim 6, although also written in independent form, is not allowable for the following reason: Applicant's traverse starts with the observation that the gate electrode of the second MOS transistor is not connected to a source/drain region of the first transistor. Actually, the gate electrode of the second MOS transistor *is* connected to a source/drain region of the first transistor in one of the Figures 2, namely: Figure 2A (cf. also col. 5, l. 55-68). Because examiner referred to Figure 2 rather than more specifically Figure 2A the rejection here will be repeated with the replacement of the reference to Figure 2 by the reference to Figure 2A. Because indeed the gate electrode of the second MOS transistor *is* connected to a source/drain region of the first transistor in one of the Figures 2, namely: Figure 2A, Keown et al is indeed capable of directly observing fluctuation in potential of the gate electrode of one transistor by using a pn junction in the other transistor as admitted by Applicant in said Remarks.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 6*** is rejected under 35 U.S.C. 102(b) as being anticipated by Keown et al (5,286,656). Keown et al teach (cf. Figure 2A and col. 5, l. 55-68) a semiconductor device comprising:

a) a second MOS transistor (either TPMOS or TNMOS depending on whether the substrate of wafer is N-type or P-type), including a portion (S of TNMOS in case second MOS transistor is TNMOS; D of TPMOS in case second MOS transistor is TPMOS) that *can* be measured by a fluctuation in a potential;

b) a wire having a first end and second end (wire connecting S of TNMOS and D of TPMOS), the second end being connected with said portion that can be measured; and

c) an observation part including a pn junction *that can be* irradiated with a laser beam to detect said fluctuation in potential, wherein:

1) said observation part includes a first MOS transistor (the other of the TPMOS and TNMOS transistors that is NOT said second MOS transistor) having:

i) a source/drain region (D of TPMOS if TPMOS is said first transistor, and S of TNMOS if TNMOS is said first MOS transistor) including a first impurity region of first conductivity type (P-type for TPMOS, N-type for TNMOS), that is connected to said first end of said wire and that is formed within a second impurity region of second impurity type (N-type for TPMOS as first MOS transistor, P-type for TNMOS as first MOS transistor); and

ii) a gate electrode that is electrically insulated from a gate electrode of said second MOS transistor (please note that the gate of the TNMOS transistor is connected to a test voltage outlet DBP1 while the gate of the TPMOS transistor is connected to another test voltage outlet DBP2, while "respective test voltages are applied at test bond pads DBP1 and DBP2: hence these test voltages are independent and consequently DBP1 and DBP2, and hence the gates of the TNMOS and TPMOS transistors, are not electrically connected). Said portion measured is said gate electrode of said second MOS transistor, because current and voltage measurements are carried out and the current is known to be a function of gate characteristics (cf. column 5, lines 11-45), said gate electrode of said second MOS transistor being connected through said wire with said source/drain region of said first MOS transistor (see Figure 2A).

Although not specifically spelled out in Keown et al the existence of a substrate of a specific conductivity type and a well around either the TNMOS or TPMOS of opposite conductivity type depending on whether said substrate conductivity type is N-type or P-type is *inherent* in the CMOS device of Keown et al (cf. col. 4, lines 46-59)

tested according to the description (cf. column 4, line 60 –column 6, line 43 and Figure 2) in Keown et al, because in CMOS devices one transistor is an NMOS transistor and the other transistor is a PMOS transistor.

Although Keown et al do not teach ad a) that said portion *is* measured by fluctuation in potential, nor ad c) that said observation part *is* irradiated with a laser beam to detect said fluctuation in potential only the actual structure and not the use of the device is relevant to the presently elected invention (see Papers 4 and 6). Applicant is reminded that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In conclusion, Keown et al anticipate claim 6.

Allowable Subject Matter

3. ***Claim 11*** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: Keown et al do not teach that said first MOS transistor to include a third impurity region connected to said wire.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
April 23, 2004